WHAT IS CLAIMED IS:

1. A field effect transistor, comprising:

a semiconductor substrate of a first conductivity type;

a gate insulation film formed on said semiconductor substrate;

a gate electrode formed on said gate insulation film;

a source electrode and a drain electrode formed at lateral sides, respectively, of said gate electrode;

a source region of a second conductivity type which is in contact with said source electrode;

a drain region of the second conductivity type which is in contact with said drain electrode;

a punch-through stopper layer of the first conductivity type formed in contact with said source region at a location deeper than a junction between said source region of the second conductivity type and said semiconductor substrate of the first conductivity type in such a gate overlap structure that said punch-through layer penetrates from beneath an end face of said gate insulation film adjacent to said source electrode toward said drain electrode in contact with said gate insulation film; and

a field relaxation layer of the second conductivity type formed in contact with said drain region in such a gate overlap structure in which said

field relaxation layer penetrates from beneath an end face of said gate insulation film adjacent to said drain electrode toward said source electrode in contact with said gate insulation film;

wherein a high-density layer of the second conductivity type which is in contact with said source electrode and a high-density layer of the second conductivity type which is in contact with said drain electrode are disposed at both sides, respectively, of said gate electrode without being in contact with said gate insulation film.

2. A field effect transistor, comprising:

a semiconductor substrate of a first conductivity type;

a gate insulation film formed on said semiconductor substrate;

a gate electrode formed on said gate insulation film;

a source electrode and a drain electrode formed at lateral sides, respectively, of said gate electrode;

a source region of a second conductivity type which is in contact with said source electrode;

a drain region of the second conductivity type which is in contact with said drain electrode; and

a field relaxation layer of the second conductivity type formed in contact with said drain region in such a gate overlap structure that said field

relaxation layer extends from beneath an end face of said gate insulation film adjacent to said drain electrode toward said source electrode in contact with said gate insulation film;

wherein said field relaxation layer penetrates from beneath an end face of a gate electrode side wall toward said source electrode for a distance of at least 0.15 μm.

3. A field effect transistor according to claim 1,

wherein said field relaxation layer penetrates from beneath an end face of a gate electrode side wall toward said source electrode for a distance of at least 0.15 μm.

4. A field effect transistor according to claim 1,

further comprising:

a layer of the first conductivity type formed on a surface of the field relaxation layer of the second conductivity type and/or alternatively a drain region of the second conductivity type.

5. A field effect transistor according to claim 1,

further comprising:

an impurity layer of the first conductivity type or alternatively the second conductivity type formed on a surface of said semiconductor substrate extending beneath said gate insulation film.

6. A method of manufacturing a semiconductor device including a field effect transistor comprised of a semiconductor substrate of a first conductivity type, a gate insulation film formed on said semiconductor substrate, a gate electrode formed on said gate insulation film, a source electrode and a drain electrode formed on lateral sides, respectively, of said gate electrode, a source region of a second conductivity type which is in contact with said source electrode and a drain region of the second conductivity type which is in contact with said drain electrode,

said method comprising the steps of:

forming in the semiconductor substrate having formed thereon the gate insulation film a punch-through stopper layer of the first conductivity type in such a gate overlap structure that said punch-through layer penetrates from beneath an end face of said gate insulation film adjacent to said source electrode toward said drain electrode;

forming a field relaxation layer of the second conductivity type in such a gate overlap structure that said field relaxation layer penetrates from beneath an end face of said gate insulation film adjacent to said drain electrode toward said source electrode;

forming a gate electrode;

forming a low-density impurity layer of the second conductivity on the source electrode or

alternatively on the whole surface of the substrate by using said gate electrode as a mask;

forming side walls of insulation films on lateral surfaces, respectively, of said gate electrode by removing an insulation film by dry-etching after deposition of said insulation films; and

forming a high-density impurity layer of the second conductivity on the whole surface of the substrate by using said gate electrode and said lateral walls as the mask.

7. A method of manufacturing a semiconductor device including at least a field effect transistor which is comprised of a semiconductor substrate of a first conductivity type, a gate insulation film formed on said semiconductor substrate, a gate electrode formed on said gate insulation film, a source electrode and a drain electrode formed on lateral sides, respectively, of said gate electrode, a source region of a second conductivity type which is in contact with said source electrode and a drain region of the second conductivity type which is in contact with said drain electrode,

said method comprising the steps of:

forming in the semiconductor substrate having formed thereon the gate insulation film a punch-through stopper layer of the first conductivity type by using said gate electrode as a mask such that said punch-through layer penetrates said semiconductor substrate

beneath said gate insulation film from underneath an end face of said gate electrode adjacent to said source electrode with an angle of incidence of at least 10° relative to an interface between said gate insulation film and said semiconductor substrate;

forming a field relaxation layer of the second conductivity type by using said gate electrode as a mask such that said field relaxation layer penetrates said semiconductor substrate beneath said gate insulation film from underneath an end face of said gate electrode adjacent to said drain electrode with an angle of incidence of at least 10° relative to interface between said gate insulation film and said semiconductor substrate;

forming a low-density impurity layer of the second conductivity on the source electrode or alternatively on the whole surface of the substrate by using said gate electrode as a mask;

forming side walls of insulation films on lateral surfaces, respectively, of said gate electrode by removing an insulation film by dry-etching after deposition of said insulation films; and

forming a high-density impurity layer of the second conductivity on the whole surface of the substrate by using said gate electrode and said lateral walls as the mask.